REMARKS

Claims 1-24 are pending in this application. In the Office Action dated September 16, 2003, the Examiner took the following action: (1) rejected claims 1-24 under 35 U.S.C. § 103(a) as being obvious over either U.S. Patent No. 5,673,005 to Pricer, U.S. Patent No. 5,550,783 to Stephens, Jr. *et al.*, U.S. Patent No. 5,229,929 to Shimizu *et al.*, U.S. Patent No. 5,182,524 to Hopkins, U.S. Patent No. 5,130,565 to Girmay or U.S. Patent No. 4,746,996 to Furuhata *et al.*

The disclosed embodiments of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter. These differences were discussed with the Examiner during the February 26, 2003 interview in which the Examiner agreed that all of the claims patentably distinguished over the cited references. Unfortunately, the Examiner did not retain notes or prepare an Interview Summary Record, and the response was apparently lost for a considerable period, so that the Examiner does not recall the basis for his agreement that all of the claims are patentable.

The invention described in the application is directed to solving the problem of precisely coupling digital signals, such as data, from a memory device to a memory controller. As the speed of memory devices continues to increase, controlling the timing at which data signals are received at the memory controller becomes more critical. Precisely controlling the timing at which data signals are received by a memory controller is even more difficult where, as in the disclosed embodiment, the memory controller communicates with several memory devices. In such cases, the timing of data signals generated by each memory device may be different and the time required for the data signals to propagate from each memory device may vary. In short, the disclosed invention is directed to solving a particular problem incurred in *coupling read data from a memory device to a memory controller.*

The disclosed embodiment of applicant's invention solves the above-described problem by (1) determining at the memory controller the timing error at which a digital signal, such as read data, is received by the memory controller from a memory device, (2) communicating the existence and/or magnitude of the error to the memory device that outputted the digital signal, and (3) adjusting the timing at which the next digital signal is output from the memory device so that the timing error at which it is received at the memory controller is reduced. Note that the timing adjustment is done at the memory device rather than at the memory controller, even though it is the timing of the digital signal at the memory controller that is critical. Thus, the memory device adapts itself to output the digital signal to the memory controller at the optimum time for the memory controller to capture the digital signal. This feature, which may be termed "adaptive signal timing", allows a memory system containing the memory controller and several memory devices to automatically configure itself for optimum performance.

In the disclosed embodiment, the memory controller generates a master clock signal that is coupled from the memory controller to the memory device. The memory device then uses the master clock signal to generate an echo clock signal. The phase of the echo clock signal relative to the master clock signal is determined by timing control data that is received from the memory controller. The echo clock signal is used to clock read data from the memory device, and this read data, as well as the echo clock, are coupled from the memory device to the memory controller. The memory controller then compares the phase of the received echo clock signal to the phase of the master clock signal to determine the timing error of the echo clock signal. Since the echo clock signal is used to clock the read data, the timing error of the echo clock signal also corresponds to the timing error of the read data as it is received by the memory controller. The memory controller sends timing control data indicative of the timing error to the memory device, and the memory device then adjusts the phase of the error clock signal relative to the phase of the received master clock signal accordingly. This timing adjustment reduces the timing error of the echo clock signal and the read data as they are received at the memory controller. As a result, the master clock signal has the proper phase to clock the read data into the memory controller from several different memory devices that may have different propagation delays from the memory devices to the memory controller.

It should be recognized that the individual components of the disclosed system and method may be conventional. For example, it is admittedly conventional to use a clock signal to clock read data into a memory controller. It is also conventional to compare two clock signals to each other to provide a phase error signal. However, what is not conventional is to use these and other components in combination to provide this "adaptive signal timing," for ensuring that digital signals coupled from a memory device to a memory controller are received at the memory controller in synchronism with a clock signal that is present in the memory controller, as explained above.

None of the references cited in the Office Action suggest this adaptive signal timing concept for digital signals coupled from a memory device to a memory controller. The patent to Pricer does not even relate to memory devices, memory controllers or techniques for coupling signals between memory devices and a memory controller. Instead, the Pricer patent merely teaches a delay lock loop for generating a clock signal having substantially the same phase as an input clock signal. While the Pricer patent may teach determining a timing error between two digital signals, it does not teach or even begin to suggest performing that function in a memory controller, then communicating the existence and/or magnitude of the error to a memory device that provided one of the digital signals, and then adjusting the timing at which the next digital signal is output to the memory controller from the memory device so that the timing error at which the digital signals is received at the memory controller is reduced. In fact, the Office Action admits the Pricer patent does not teach even the basic concept of the invention, *i.e.*, creating a feedback loop between a memory device and a memory controller so that digital signals output from the memory device are received by the memory controller at the proper time. In this regard, it is simply not proper to dismiss the basic concept of the invention as being obvious to one skilled in the art absent a prior art reference showing that concept. Indeed, if the basic concept is so obvious, there should be no difficulty in finding a prior art reference that discloses it.

The patent to Stephens, Jr., *et al.* likewise fails to suggest the basic concept of applicant's system and method. Instead, the Stephens, Jr., *et al.* patent teaches only the use of a phase-lock loop to provide a clock signal for a memory device. Significantly, the entire loop, including the feedback path for the loop, is contained within a single memory device. Thus, the

Stephens, Jr., *et al.* patent does not suggest the above describe "adaptive signal timing" concept for coupling digital signals from a memory device to a memory controller with the proper phase relationship to a clock signal in the memory controller.

The patent to Shimizu *et al.* is even less relevant that the patent to Pricer and the patent to Stephens, Jr., *et al.* because it does not even compare the phase or timing of two signals. Instead, "[t]he differential amplifier 17 correct the *level* of the sine wave reference signal supplied from the sine wave generator 14 by the signal supplied from the detecting circuit 13, and outputs a corrected sine wave reference signal." [Column 6, lines 31-35, emphasis added]. Thus, the circuitry that is considered to be a "comparator" compares signal levels, *i.e.*, signal amplitudes, not signal phases. Furthermore, the disclosed circuitry is used in an inverter to generate AC power for DC power rather than in a memory device or memory controller.

The patent to Hopkins, like all of the other references except for the patent to Stephens, Jr., *et al.*, does not even relate to memory devices or memory controllers. Instead, the patent to Hopkins merely discloses a closed-loop control system for controlling the amplitude and phase of a signal generated by a high power pulsed microwave amplifier. The problem that the disclosed circuit addresses is that the pulses are too short to detect the amplitude and phase of the pulses using conventional means. The Hopkins circuit does not relate to adjusting the phase of digital signals transmitted by a first digital device (*e.g.*, a memory device) so that they are received with a phase that matches a clock signal at a second digital device (*e.g.*, a memory controller). Thus, the patent to Hopkins does not suggest even the basic concept of applicant's "adaptive signal timing" concept.

The patent to Girmay discloses a pulse width modulator ("PWM") that uses a feedback control system to control the duty cycle of an output signal generated by the PWM. The duty cycle of a signal generated by the current controlled PWM is compared by a summer "Σ" to the duty cycle of a reference signal generated by a PMW reference generator. Thus, the Girmay circuit does not even compare the timing of two signals at a memory controller or in any other type of device.

The patent to Furuhata *et al.* discloses a signal skew error correction circuit for television receivers in which a phase-lock loop is used to phase-lock the output of a voltage-controlled oscillator 407 to a reference signal generated by a crystal oscillator 408. As the

Examiner recognizes, the Furuhata *et al.* patent does not disclose a memory controller that senses a timing error of a digital signal generated by a memory device, and then couples information about the timing error from the memory controller to a memory device which the memory device uses to adjust the timing at which the next digital signal is output to the memory controller thereby reducing the timing error at the memory controller.

Turning, now, to the claims, all of the claims in the application are clearly patentable over the cited references. For example, claim 1 specifies a method of adjusting data timing in a memory system having a memory device and a memory controller. According to the claimed method, an initial output timing at the memory device is established and is then subsequently revised. The output timing is revised by "transmitting a echo clock signal from the memory device to the memory controller according to the initial output timing." After the echo clock signal is received at the memory controller, the memory controller identifies "a phase difference of the received echo clock signal relative to a timing reference signal" and "transmits control data to the memory device for revising the initial output timing in response to the identified phase difference to produce a revised output timing." Thereafter, the memory device revises the initial output timing according to the control data. The memory device then transmits data from the memory device to the memory controller according to the revised output timing.

Claim 20 is somewhat similar to claim 1 in that is specifies establishing an initial output timing at the memory device. This initial output timing is subsequently revised by "transmitting a first digital signal from the memory device to the memory controller according to the initial output timing." After the first digital signal is received at the memory controller, the memory controller identifies "a phase difference of the received first digital signal relative to a timing reference signal" and "transmits an adjustment signal to the memory device for revising the initial output timing in response to the identified phase difference to produce a revised output timing." After the memory device has revised the initial output timing according to the adjustment signal, the memory device transmits a second digital signal from the memory device to the memory controller according to the revised output timing.

As explained above, none of the cited references disclose a memory controller that identifies a phase error between a digital signal received from a memory device relative to a timing reference signal, as recited in claims 1 and 20. Nor do any of the cited references disclose

a system that transmits control data or an adjustment signal to the memory device to cause the memory device to revise the initial output timing it used to transmit the digital signal. The cited references thus not only fails to include individual components that operate as claimed, but these components do not operate together in any manner that is at all similar to the methods of claims 1 or 20.

Claim 6 is directed to a method of controlling data flow in a memory system that includes a memory controller and a memory device. A master clock signal and a first read command are transmitted from the memory controller to the memory device. In response to the first read command, the memory device produces a first set of data and an echo signal that has a phase shift relative to the master clock signal. The first set of data and the echo signal are transmitted to the memory controller, which compares the received echo signal to the master clock signal and selects an adjusted time delay in response to the comparison. The memory controller then issues a second read command, which cases the memory device to provide and a second set of data. This second set of data are transmitted to the memory controller with the adjusted time delay. As explained above, none of the cited references disclose or suggest this "adaptive signal timing" method, which allows read data to be received at a memory controller in synchronism with a master clock signal.

Claims 10 and 13 are directed to a memory controller and a memory system, respectively. The memory controller of claim 10 includes a phase comparing circuit that produces a phase signal in response to a phase difference between an echo signal received from a memory device and a master clock signal generated by a master clock source in the memory controller. Claim 10 further specifies a logic circuit that produces adjustment data in response to the phase signal, and a control data circuit that produces a command signal in response to the adjustment data. As explained above, none of the cited references disclose or suggest a memory controller having these components or operating in this manner.

The memory system of claim 13 includes, *inter alia*, a memory controller and a memory device. The memory controller includes most of the components of the memory controller of claim 10, and the memory device includes an echo signal generator that generates the echo signal responsive to the master clock signal received from the memory controller. The claimed memory device also includes a data latch that is responsive to a control signal to

transmit data to a data bus. Finally, the memory device includes a variable delay circuit that is responsive to the adjust command on the command bus to produce the control signal at a time corresponding to the adjust command produced by the memory controller. The Examiner has not even attempted to show where most of these components are found in the cited references, and the systems disclosed in the cited references clearly do operate in the manner specified by claim 13.

Claim 16 is directed to a method of adjusting data timing in a memory system having a memory device and a memory controller. A first set of data is transmitted to the memory device according to a first clock signal, and the memory device then establishes an initial output timing having a default phase relationship with the first clock signal. This initial output timing is used to transmit a second set of data from the memory device to the memory controller. The memory controller compares the phase of the second set of data to the phase of the first clock signal to identify a phase error. The identified phase error is then used to revise the initial output timing, and the memory controller transmits a third set of data from the memory controller to the memory device for allowing the memory device to revise the initial output timing at the memory device to produce a revised output timing. Again, none of the cited references disclose or suggest the subject matter of claim 16.

The claims that are dependent on the above-discussed independent claims also patentably distinguish over the cited references because of their dependency on patentable independent claims and because of the additional limitations added by those claims.

The Examiner has asserted, and the applicant agrees, that most of the cited references disclose a feedback control system using a delay-lock loop or a phase-lock in which the timing or phase of two signals are compared to each other. The Examiner is apparently taking the position that applicant's use of a delay-lock loop or a phase-lock loop for the specific application claimed would have been obvious simply because delay-lock loops and phase-lock loops are known. Not only is this approach contrary to law, but it is also contrary to the decisions that led to the issuance of the patents used as cited references, all of which cover specific uses of delay-lock loops and phase-lock loops despite the fact that such loops were known at the time the applications for those patents were filed. Yet, in those cases, the specific

uses for delay-lock loops and phase-lock loops were not considered obvious simply because delay-lock loops and phase-lock loops were known.

Finally, the claims are being amended to place them in better form. None of these amendments are considered to alter the scope of any of the claims except for the broadening amendments to claim 3, 4 and 23.

All of the in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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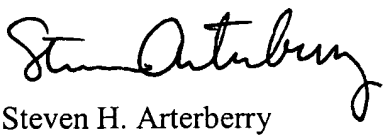

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